REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on May 30, 2003. Claims 7 and 23 are amended. Claims 1-84 remain pending in this application.

Objection to the Disclosure

The disclosure was objected to for not describing Figs. 9-12 and 14 as Prior Art. Applicant respectfully traverses. With respect to Fig. 9, the specification states: *This graph is provided herein to illustrate the known relationship between the silicon amount and the refractive index.* Specification at page 21, lines 6-7. With respect to Fig. 10, the specification states: *This graph is provided herein to illustrate the known relationship between the amount of silicon and the conductivity of the film.* Specification at page 21, lines 15-16. With respect to Fig. 11, the specification states: *Figures 11 and 12 provide graphs that illustrate the known relationship between the flatband shift and applied fields for films having varying percentages of excess silicon as represented by the SiH_2Cl_2/NH_3 flow rate ratio R.* Specification at page 21, lines 21-22. With respect to Fig. 14, the specification states: *Figure 14 is a cross-section view of a conventional nonvolatile field effect transistor (NV FET) device.* Specification at page 24, lines 8-9. Applicant respectfully requests withdrawal of the rejection.

Claim Objections

Non-elected claims 85-88 were objected to for not being canceled. Applicant notes that claims 85-88 were previously canceled in the Response to Restriction Requirement dated April 11, 2003. Applicant respectfully requests withdrawal of the objection.

§112 Rejection of the Claims

Claim 7 was rejected under 35 USC § 112, second paragraph. Claim 7 has been amended to further clarify the recited subject matter. Applicant respectfully requests withdrawal of the §112 rejection, and reconsideration and allowance of the claims.

§103 Rejection of the Claims

Claims 1-84 were rejected under 35 USC § 103(a) as being unpatentable over Hong et al. (U.S. 5,445,984) in view of Kato et al. (U.S. 4,495,219), Bertin et al. (U.S. 5,617,351), Bass, Jr. et al. (U.S. 4,870,470), Wolf et al. (U.S. 4,717,943), Nguyen et al. (U.S. 5,510,278), and Forbes (U.S. 5,852,306). Applicant respectfully traverses the rejection for at least the following reasons.

The office action did not make out a prima facie case of obviousness because the claimed subject matter has not been considered as a whole, and because the cited references do not recognize the problem solved by the claimed subject matter. The present subject matter relates to nonvolatile memory devices that incorporate a band-gap engineered gate stack with asymmetric tunnel barriers such that the memory device is capable of being programmed primarily through charge transport between the control gate and the floating charge-storage medium. Specification at page 10 lines 5-16. The band-gap engineered gate stack with asymmetric tunnel barriers is provided by the combination recited in the claims. Applicant respectfully asserts that the references relied upon in the rejection fails to provide a suggestion or motivation to combine the references and apply the combination of references to solve a same or similar problem which is addressed by the gate stack with asymmetric tunnel barriers.

With respect to independent claim 1, Applicant is unable to find, among other things, in the cited portions of the references a motivation to combine the references to form a gate stack for a nonvolatile memory cell that comprises a Silicon Dioxide (SiO_2) layer in contact with a channel region of the memory cell, a Tantalum Oxide (Ta_2O_5) layer in contact with the SiO_2 layer, a charge-storage region in contact with the Ta_2O_5 layer, and a Zirconium Oxide (ZrO_2) layer in contact with the charge-storage layer, as recited in the claim. Dependent claims 2-7 depend on independent claim 1, and are believed to be patentable at least for the reasons provided with respect to claim 1.

With respect to independent claim 8, Applicant is unable to find, among other things, in the cited portions of the references a motivation to combine the references to form a gate stack for a nonvolatile memory cell, comprising a Silicon Dioxide (SiO_2) layer in contact with a channel region of the memory cell, a Tantalum Oxide (Ta_2O_5) layer in contact with the SiO_2 layer, a charge-trapping floating plate in contact with the Ta_2O_5 layer, and a Zirconium Oxide (ZrO_2) layer in contact with the charge-storage layer, as recited in the claim. Dependent claims

9-15 depend either directly or indirectly on independent claim 8, and are believed to be patentable at least for the reasons provided with respect to claim 8.

With respect to independent claim 16, Applicant is unable to find, among other things, in the cited portions of the references a motivation to combine the references to form a nonvolatile memory cell, comprising a first source/drain region and a second source/drain region separated by a channel region in a substrate, a control gate of predetermined metallurgy, and a gate stack separating the control gate from the channel region where the gate stack includes a first insulator region including a Silicon Dioxide (SiO_2) layer and a Tantalum Oxide (Ta_2O_5) layer, a floating charge-storage region separated from the channel region by the first insulator region, and a second insulator region including a Zirconium Oxide (ZrO_2) layer, wherein the control gate is separated from the floating charge-storage region by the second insulator region as recited in the claim. The claim also recites that the gate stack includes selected material for providing desired asymmetric energy barriers in conjunction with the control gate of predetermined metallurgy, and that the desired asymmetric energy barriers are adapted to primarily restrict carrier flow during programming to a selected carrier between the control gate and the floating charge-storage region, and retain a programmed charge in the floating charge-storage region. Applicant is unable to find a showing or suggestion this language in the claim. Dependent claims 17-24 depend either directly or indirectly on independent claim 16, and are believed to be patentable at least for the reasons provided with respect to claim 16.

With respect to independent claim 25, Applicant is unable to find, among other things, in the cited portions of the references a motivation to combine the references to form a nonvolatile memory cell, comprising a p – substrate, a first n type source/drain region and a second n type source/drain region separated by a channel region in the substrate, a Silicon Dioxide (SiO_2) layer in contact with the channel region, a Tantalum Oxide (Ta_2O_5) layer in contact with the SiO_2 layer, a charge-storage region in contact with the Ta_2O_5 layer, a Zirconium Oxide (ZrO_2) layer in contact with the charge-storage layer, and an Aluminum control gate in contact with the ZrO_2 layer, as recited in the claim. Dependent claims 26-33 depend on independent claim 25, and are believed to be patentable at least for the reasons provided with respect to claim 25.

With respect to independent claim 34, Applicant is unable to find, among other things, in the cited portions of the references a motivation to combine the references to form a nonvolatile

memory cell, comprising a first source/drain region and a second source/drain region separated by a channel region in a substrate, a control gate of predetermined metallurgy, a gate stack separating the control gate from the channel region where the gate stack includes a first insulator region including a Silicon Dioxide (SiO_2) layer and a Tantalum Oxide (Ta_2O_5) layer, a floating plate separated from the channel region by the first insulator region, the floating plate including silicon nano crystals, and a second insulator region including a Zirconium Oxide (ZrO_2) layer, wherein the control gate is separated from the floating charge-storage region by the second insulator region, as recited in the claim. The claim also recites that the gate stack includes selected material for providing desired asymmetric energy barriers in conjunction with the predetermined metallurgy of the control gate, and that the desired asymmetric energy barriers are adapted to primarily restrict carrier flow during programming to a selected carrier between the control gate and the floating charge-storing region, and retain a programmed charge in the floating charge-storage region. Applicant is unable to find a showing or suggestion this language in the claim. Dependent claims 35-41 depend either directly or indirectly on independent claim 34, and are believed to be patentable at least for the reasons provided with respect to claim 34.

With respect to independent claim 42, Applicant is unable to find, among other things, in the cited portions of the references a motivation to combine the references to form a nonvolatile memory cell, comprising a first source/drain region and a second source/drain region separated by a channel region in a substrate, a control gate, and a gate stack separating the control gate from the channel region where the gate stack includes a first insulator region, a floating charge-storage region separated from the channel region by the first insulator region, and a second insulator region, wherein the control gate is separated from the floating charge-storage region by the second insulator region. The claim also recites that a hole energy barrier from the control gate to the second insulator region is sufficiently small such that a primary programming charge transport includes hole transport from the control gate to the floating charge-storage region upon application of a programming electromotive force (EMF) at the control gate that is positive with respect to the substrate. Applicant is unable to find a showing or suggestion this language in the claim. Dependent claims 43-53 depend either directly or indirectly on independent claim 42, and are believed to be patentable at least for the reasons provided with respect to claim 42.

With respect to independent claim 54, Applicant is unable to find, among other things, in the cited portions of the references a motivation to combine the references to form a nonvolatile memory cell, comprising a first source/drain region and a second source/drain region separated by a channel region in a substrate, a control gate, and a gate stack separating the control gate from the channel region where the gate stack includes a first insulator region, a floating charge-storage region separated from the channel region by the first insulator region, and a second insulator region, wherein the control gate is separated from the floating charge-storage region by the second insulator region. The claim further recites that a hole energy barrier from the floating charge-storage region to the second insulator region and the equivalent oxide thicknesses of the second insulator region and the first insulator region are such that hole transport from the floating charge-storage region to the control gate is encouraged if an EMF transient is present at the substrate that is positive with respect to the control gate. Applicant is unable to find a showing or suggestion this language in the claim. Dependent claims 55-63 depend either directly or indirectly on independent claim 54, and are believed to be patentable at least for the reasons provided with respect to claim 54.

With respect to independent claim 64, Applicant is unable to find, among other things, in the cited portions of the references a motivation to combine the references to form a nonvolatile memory cell, comprising a first source/drain region and a second source/drain region separated by a channel region in a substrate, a control gate, and a gate stack separating the control gate from the channel region where the gate stack includes a first insulator region having a first equivalent oxide thickness, a floating charge-storage region separated from the channel region by the first insulator region, and a second insulator region having a second equivalent oxide thickness, wherein the control gate is separated from the floating charge-storage region by the second insulator region, as recited in the claim. The claim further recites that the equivalent oxide thickness of the first insulator region and the equivalent oxide thickness of the second insulator region is such that an electric field across the second insulator region is enhanced when a programming potential is applied across the control gate and the substrate, that the first insulator region and the second insulator region include materials that provide desired asymmetric energy barriers, and that the desired asymmetric energy barriers are adapted to primarily restrict carrier flow during programming to a selected carrier between the control gate

and the floating charge-storage region, and retain a programmed charge in the floating charge-storage region. Applicant is unable to find a showing or suggestion this language in the claim. Dependent claims 65-67 depend either directly or indirectly on independent claim 64, and are believed to be patentable at least for the reasons provided with respect to claim 64.

With respect to independent claim 68, Applicant is unable to find, among other things, in the cited portions of the references a motivation to combine the references to form a flash memory array, comprising a number of source lines, a number of control gate lines, a number of bit lines, and a number of nonvolatile memory cells, where each nonvolatile memory cell includes a p – substrate, a first n type source/drain region and a second n type source/drain region separated by a channel region in the substrate, a Silicon Dioxide (SiO_2) layer in contact with the channel region, a Tantalum Oxide (Ta_2O_5) layer in contact with the SiO_2 layer, a charge-storage region in contact with the Ta_2O_5 layer, a Zirconium Oxide (ZrO_2) layer in contact with the charge-storage layer, and an Aluminum control gate in contact with the ZrO_2 layer, as recited in the claim. Dependent claims 69 -76 depend on independent claim 68, and are believed to be patentable at least for the reasons provided with respect to claim 68.

With respect to independent claim 77, Applicant is unable to find, among other things, in the cited portions of the references a motivation to combine the references to form an electronic system, comprising a processor, and a memory device adapted to communicate with the processor where the memory device includes an array of flash memory cells that include a number of source lines, a number of control gate lines, a number of bit lines, and a number of nonvolatile memory cells, where each nonvolatile memory cell includes a p – substrate, a first n type source/drain region and a second n type source/drain region separated by a channel region in the substrate, a Silicon Dioxide (SiO_2) layer in contact with the channel region, a Tantalum Oxide (Ta_2O_5) layer in contact with the SiO_2 layer, a charge-storage region in contact with the Ta_2O_5 layer, a Zirconium Oxide (ZrO_2) layer in contact with the charge-storage layer, and an Aluminum control gate in contact with the ZrO_2 layer, as recited in the claim. Dependent claim 78 depends on independent claim 77, and is believed to be patentable at least for the reasons provided with respect to claim 77.

With respect to independent claim 79, Applicant is unable to find, among other things, in the cited portions of the references a motivation to combine the references to provide a method

of forming a floating gate transistor, comprising forming a gate stack over the channel region, where forming a gate stack over the channel region includes forming an SiO_2 layer on the channel region, forming a Ta_2O_5 layer on the SiO_2 layer, forming a floating charge-storage region on the Ta_2O_5 layer, and forming a ZrO_2 layer on the floating charge-storage region, as recited in the claims. Dependent claims 80-84 depend on independent claim 79, and are believed to be patentable at least for the reasons provided with respect to claim 79.

Applicant respectfully requests withdrawal of the rejection, and reconsideration and allowance of the claims.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 373-6960) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 2nd day of September, 2003.

Amy Moriarty _____

Name Signature